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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Akira Nishiyama

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EXAMINER

MAI, ANH D

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/891,129

Applicant(s)

NISHIYAMA ET AL.

Examiner

Anh D. Mai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,4,6-9,12-18 and 20-28 is/are pending in the application.
- 4a) Of the above claim(s) 14 and 15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,4,6-9,12,13,16-18 and 20-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Status of the Claims

1. Amendments filed December 15, 2003 has been entered. Claims 2 and 19 have been canceled. Claim 4 has been amended. Claims 27 and 28 have been added. Claims 1, 3,4, 6-9 12-18 and 20-28 are pending. Claims 14 and 15 have been withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-4, 7-9, 12, 13, 16-19 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anthony et al., (J.P Patent No. 11-135774) in view of Applicant's Attachment (filed June 6, 2003) or M.R. Visokay et al., all of record (IDS Paper No. 8).

With respect to claim 1, Anthony teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (20); and

a circuit element using an insulating film (36) formed in the semiconductor substrate (20), the insulating film (36) containing a silicon compound containing oxygen, and a metal compound containing a metal other than silicon and oxygen, the insulating film (36) further comprising crystals. (See Fig. 8, page 27, line 14-page 28, line 14).

Anthony is shown to teach all the features of the claim with the exception of explicitly disclosing the size of the nano-crystals.

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However, Anthony clearly teaches that the silicate 36 is subjected to a high temperature anneal to densify or *crystallize* (page 28, lines 5-7).

Applicant's Attachment (Fig. (a)) and Visokay (Fig. 3b) disclose the diameter of the crystals of the insulating film to be within the claimed range (1nm – 10nm), thus, the nano-crystals within the crystallized insulating film (36) should have sizes within the claimed range..

With respect to claim 16, Anthony teaches a semiconductor device substantially as claimed including:

- a semiconductor substrate (20);

- source and drain regions (140/160) formed apart from each other in the semiconductor substrate;

- a gate the insulating film (36) formed between the source and drain regions (140/160), the gate insulating film (36) containing a silicon compound containing oxygen, and a metal compound containing a metal other than silicon and oxygen, the insulating film (36) further comprising crystals; and

- a gate electrode (38) formed on the gate insulating film (36). (See Figs. 1 and 9, page 27, line 14-page 28, line 14).

With respect to the size of the nano-crystals, the similar reasoning as that of claim 1 also applies.

With respect to the source and drain regions, although does not explicitly disclosing in the invention, however, the gate insulating layer (36) of Anthony is intended as the substitute for

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the regular silicon oxide layer (180), thus, the structure of the MOSFET (Fig. 1) is unchanged, hence source and drain regions.

With respect to claims 3 and 18, the crystal of Anthony are made of the metal compound.

With respect to claim 4, the nano-crystal of Anthony is made of an oxide of a metal (La, Y, Ta, Hf or Zr) other than silicon.

With respect to claims 7 and 21, the semiconductor device of Anthony further includes a silicon oxynitride film formed between the semiconductor substrate and the insulating film. (See page 21, ll. 23-25).

With respect to claims 8 and 22, the metal other than silicon of Anthony is at least one of metal selected from the group consisting of La, Y, Ta, Zr, Hf. (See page 23, ll. 12-24).

With respect to claim 9, the circuit element of Anthony is a MOSFET and the insulating film (36) is a gate insulating film of the MOSFET.

With respect to claims 12 and 23, Anthony teaches: near the silicon interface the silicate has a large SiO₂ component, while the upper portion of the silicate layer has a large metal oxide component. (page 16, lines 10-12). Anthony further adds: assumes that a protective or native silicon oxide region 26 (preferably comprising less than 1nm of oxide).

Note that the specification contains no disclosure of either the critical nature of the claimed: *distance of 0.7nm from the interface* of any unexpected results arising therefrom.

Where patentability is aid to based upon particular chosen dimension or upon another variable

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recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, at least one of the nano-crystals of Anthony is position away from the interface of the silicon substrate and the insulating film by a distance of *less than 1nm*, which approximate the claimed range.

With respect to claims 13 and 24, the insulating film (36) of Anthony is a mixed film containing silicon compound and metal compound.

With respect to claim 17, the silicon compound of Anthony is a compound selected from the group consisting of a silicon oxide.

With respect to claim 25, the gate electrode (38) of Anthony includes polycrystalline silicon layer.

With respect to claim 27, Anthony teaches “a graded silicate film may be formed that is mainly SiO₂ at the substrate 10 interface (e.g. 2-10 mol% metal oxide), thus providing an interface with a quality similar to that obtained with pure SiO₂. The ratio of silicon to metal is decreased with a grading profile that results preferably in a greater percentage of metal oxide near the top of the gate dielectric film” (see page (25)).

Thus, the silicon in the insulating film (36) of Anthony is at least including the claimed (15% and 80%) range.

3. Claims 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anthony '774, Applicant's Attachment and Visokay et al., as applied to claims 1 and 16 above, and further in view of Wilk (U.S. Patent No. 6,544,875) of record.

Anthony teaches the dielectric layer may be made substantially thicker than a conventional gate dielectric with equivalent field effect. (See Summary pages 15-16).

Thus, Anthony is shown to teach all the features of the claim with the exception of explicitly disclosing the thickness of the insulating layer (36).

However, Wilk teaches a high dielectric constant and low leakage dielectric material is formed to a thickness (4nm-10nm) that overlaps the claimed range (3nm-20nm). (col. 3, lines 40-57).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the insulating film (36) of Anthony to the thickness as taught by Wilk to form a high dielectric constant layer for the miniature MOSFET device.

4. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anthony '774, Applicant's Attachment and Visokay et al., as applied to claim 16 above, and further in view of Bai et al. (U.S. Patent No. 5,818,092) of record.

Anthony teaches all the features of the claim with the exception of further includes silicide layers formed on the source and drain regions (140/160).

However, Bai teaches field effect transistor (100) formed on a semiconductor substrate (101) further includes silicide layer (114) formed on the source and drain regions (110).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further includes silicide layers on the source and drain regions (140/160) of Wallace as taught by Bai to reduce sheet resistance. (See col. 1, lines 13-22).

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anthony '774, Applicant's Attachment and Visokay et al., as applied to claim 27 above, and further in view of Robert et al. (U.S. Patent No. 4,464,701).

Anthony teaches an insulating film (36) containing silicon compound and metal compound.

Thus, Anthony is shown to teach all the features of the claim with the exception of using Ti as the metal in the insulating film.

However, Robert teaches an insulating film containing a silicon and a metal from a group of transitional metals including Hf, Ta, Zr, Ti, Y and rare earth metals.

Therefore, Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Ti in the insulating film of Anthony as taught by Robert because, insulating film containing metal within the transitional metals group has a dielectric constant higher than that of SiO₂.

Response to Arguments

6. Applicant's arguments filed December 15, 2003 have been fully considered but they are not persuasive.

With respect to claim 1, Applicants argue: the temperature of annealing of 750 °C as disclosed by Anthony is not believed to result in forming nano-crystals.

Anthony clearly teaches: “a high temperature anneal of silicon layer 36 is selected to densify or crystallize the film after low temperature oxidation”. (See page (28)).

Thus, clearly the nano-crystals have been formed. As shown in Applicants’ Attachment and Visokay et al., the size of the nano-crystals after the crystallization have been determined to be within the claimed range (1 nm and 10 nm).

Further note, the instant specification also discloses that nano-crystals are formed in the temperature range of 600 °C to 1000 °C. (See Example 6).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Contrary to the Applicants assertion that no teachings in Applicants’ Attachment or Visokay can overcome the deficiencies of Anthony, the Attachment and Visokay support the size of nano-crystals formed by Anthony analytically.

The Attachment as well as Visokay show the present of nano-crystals within the crystallized insulating film.

Applicants also argue that crystallization occurs when annealing is performed at 1000 °C.

However, the instant specification clear show a contrary, wherein the crystallization occurs at 600 to 1000 °C. Note that, 1000 °C as shown n the Attachment and Visokay is to show that at such temperature, crystallization has already occurred in HfSiO, while, at same

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temperature or even higher, HfSiON of various composition maintains an amorphous state.

Thus, Attachment and Visokay confirmed sizes of the crystal within the crystallization of the insulating film of Anthony.

With respect to Visokay, Applicants appears to contend that Visokay is younger thus, can not be applied against the current pending claims.

However, the finding of Visokay and the Attachment represent a “fact”, since the nano-crystals have already existed within the crystallized insulating film 36 of Anthony.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A.M
March 1, 2004



LONG PHAM
PRIMARY EXAMINER